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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,297	02/12/2004	Guy-ho Lyu	5649-1206	5272

7590 07/12/2005

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EXAMINER
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SOWARD, IDA M

ART UNIT	PAPER NUMBER
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2822

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

18

<b>Office Action Summary</b>	<b>Application No.</b> 10/777,297	<b>Applicant(s)</b> LYU ET AL.	
	<b>Examiner</b> Ida M. Soward	<b>Art Unit</b> 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 May 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 22-31 is/are allowed.
- 6) ☒ Claim(s) 1-6, 11-15 and 19-21 is/are rejected.
- 7) ☒ Claim(s) 7-10 and 16-18 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

This Office Action is in response to the election filed May 11, 2005.

### ***Election/Restrictions***

Applicant's election without traverse of claims 1-31 in the reply filed on May 11, 2005 is acknowledged.

### ***Priority***

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Specification***

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 11-15 and 19-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Liao et al. (5,637,903).

In regard to claim 1, Liao et al. teach a semiconductor device, comprising: a semiconductor substrate 1; a plurality of isolation regions 2 in the semiconductor substrate 1 that define an active region; a gate electrode 4 & 8 on the active region, wherein the gate electrode 4 & 8 comprises a metal silicide layer 8 on a polysilicon layer 4; and a conductive layer 15 that is on, and electrically connected to, the gate electrode 4 & 8; wherein the conductive layer 15 bridges at least one gap in the metal silicide layer 8 (Figure 6, columns 3-4, lines 5-67 and 1-48, respectively).

In regard to claim 2, Liao et al. teach the conductive layer 15 directly on the metal silicide layer 8 (Figure 6, columns 3-4, lines 5-67 and 1-48, respectively).

In regard to claim 3, Liao et al. teach a gate insulation pattern 3 between the active region and the gate electrode 4 & 8 (Figure 6, columns 3-4, lines 5-67 and 1-48, respectively).

In regard to claim 4, Liao et al. teach the conductive layer 15 being a conductive line pattern (Figure 6, columns 3-4, lines 5-67 and 1-48, respectively).

In regard to claim 5, Liao et al. teach the conductive line pattern 15 formed of at least one of aluminum, tungsten, titanium, tantalum, or copper (Figure 6, column 4, lines 26-48).

In regard to claim 6, Liao et al. teach an interlayer dielectric 13 on the semiconductor substrate 1, and wherein the conductive line pattern 15 is disposed in a

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groove 14 in the interlayer dielectric (Figure 6, columns 3-4, lines 5-67 and 1-48, respectively).

In regard to claims 11 and 21, Liao et al. inherently teach the conductive layer 15 decreasing the resistance of the gate electrode 4 & 8 because the structure is the same as the claimed invention (Figure 6, columns 3-4, lines 5-67 and 1-48, respectively).

In regard to claim 12, Liao et al. teach a semiconductor device comprising: a semiconductor substrate 1; a gate line 4 & 8 including a gate insulation pattern 3 and a gate electrode 4 & 8 which are sequentially stacked on the semiconductor substrate 1; a spacer 11 formed on a sidewall of the gate line 4 & 8; and a conductive line pattern 15 disposed on the gate line 4 & 8; and wherein the conductive line pattern 15 is parallel to the gate line 4 & 8 and electrically connected to the gate electrode 4 & 8 (Figure 6, columns 3-4, lines 5-67 and 1-48, respectively).

In regard to claim 13, Liao et al. teach the gate electrode 4 & 8 comprising a doped 7 polysilicon layer 4 (Figure 6, column 3, lines 58-67).

In regard to claim 14, Liao et al. teach a metal silicide layer 8, wherein the metal silicide layer 8 is on the doped 7 polysilicon layer 4 (Figure 6, column 3, lines 85-67).

In regard to claim 15, Liao et al. teach an interlayer dielectric 13 on the semiconductor substrate 1 that includes a groove 14 that exposes a top surface of the gate line 4 & 8, and where the conductive line pattern 15 is provided in the groove 14 (Figure 6, columns 3-4, lines 5-67 and 1-48, respectively).

In regard to claim 19, Liao et al. teach the conductive line pattern 15 being made of metal (Figure 6, column 4, lines 26-48).

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In regard to claim 20, Liao et al. teach the conductive layer 15 bridges at least one gap in the metal silicide layer 8 (Figure 6, columns 3-4, lines 5-67 and 1-48, respectively).

***Allowable Subject Matter***

Claims 22-31 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not disclose, make obvious, or otherwise suggest the structure of the applicant's together with the other limitations of the independent claims, such as a first gate line and a second gate line on the semiconductor substrate and spaced apart from each other, the first gate line including a first gate electrode stacked on a first gate insulation pattern, and the second gate line including a second gate electrode stacked on a second gate insulation pattern; and a conductive line pattern on the first and second gate lines, wherein the conductive line pattern has a first portion parallel to the first gate line and a second portion parallel to the second gate line, and wherein the conductive line pattern electrically connects the first and second gate electrodes with each other. The dependent claims being further limiting and definite are also allowable.

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Claims 7-10 and 16-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### ***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to semiconductor devices:

Gonzalez (US 2002/0119640 A1)      Ohno (5,621,232)  
Simacek et al. (US 2004/0119113 A1)      Yamamoto et al. (US 6,359,318 B1)  
Yoshida et al. (US 6,528,826 B2).

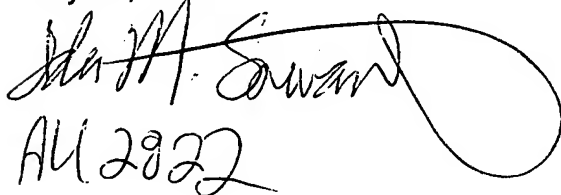
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS  
July 10, 2005

  
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